REMARKS

The present Office Action rejects claims 1-27 in view of the prior art. Applicant respectfully traverses this rejection and provides the following explanation.

The cited prior art utilizes the crossbar to accelerate the apparent memory access performance by interlacing the memory banks and pipelining the memory access cycles stages, whereas the present invention utilizes the circuit switched crossbar architecture to uniquely accommodate slow speed peripherals in the midst of high speed memory devices to improve overall system performance and efficiency where both slow and fast devices must coexist within a super integrated system-on-chip application. Applicant believes this concept is unique and non-obvious in view of the prior art, and presents the following detailed analysis. The cited prior art utilizes the crossbar to resolve and improve effective processor/cache performance by utilizing interlaced memory blocks and pipelined memory accesses to stagger the memory access cycle stages to hide the memory access wait cycles.

Section 102 Rejections

The Office Action rejects claims 1-3, 8-9, 11-13, 18-19, 21-22, 24-25 and 27 under 35 U.S.C. 102(e) as anticipated by (USPN 6,636,933, MacLellan). Although MacLellan's patent speaks about a crossbar controller for memory subsystems, the implementation details show the serialized packet switching network (Fig. 2A/B) on a cache memory backplane application (Fig. 3) which does not include the crossbar memory architecture of the present application to improve the system cost and performance. The MacLellan computer system describes a computer system with multiple banks of "dual-ported memory" (MA1 and MB1 of Fig. 8B) for "dual-processor" (121) architecture as shown in Fig. 8B of MacLellan. What is not described is how to make the "dual-ported memory" (R1..R4 on Fig. 9C) and how to expand it for a "multi-

ported cross-bar memory" for "multi-hosted-system" applications which the present application describes in detail.

Claims 1, 11, and 21 of the present application differ from the MacLellan computer system in that the present application provides a "circuit switched crossbar bus" that directly and concurrently connects any one of the hosts to any other client memory blocks for a non-blocking single cycle memory access. In contrast, the MacLellan computer system provides a "packet switched crossbar network" to allow multiple processors (120 of fig. 2) to access multiple disk drives (140 of fig .2) where the crossbar (260 of fig. 2) provides the message network switching and the "global cache memory buffer" (220 of fig. 2) provides the data packet buffering.

MacLellan's patent (col. 14, lines 35-40, 57 to col. 15, line 5), speaks of crossbar switches (5004), but line 41-56 of col. 14 describes the formation of an "information cycle" consisting of a "plurality of 16 bit words, each word being associated with a clock pulse" where 8 words (clocks) are used for control information and 4 to 256 words (clocks) are used for data packets. Consequently, MacLellan's crossbar implementation does not directly connect the host and the clients together, but rather passes the control-data packets (Fig. 2A and Fig. 2B) from one of the hosts (120) to one of the clients (140) via dedicated buffer memory blocks (220 of FIG. 8A).

MacLellan's patent (col. 14, line 57 etc. to col. 15, lines 1-5) speaks of multi-ported crossbar switches (5004 of FIG. 9B) for a multi-ported memory (R1-R4 of FIG. 9C) via dual ported memory controller (5010 of Fig. 9B), but fails to describe the crucial implementation details for the multi-ported memory (R1-R4 of Fig. 9C), describing it as just being "coupled to different control ports PA and PB of the memory array region" (col. 15, lines 30-32) of a customary fault-tolerant dual ported memory with redundant control ports as defined under US

Patent No. 5,943,287 (col. 15, lines 43-46). However, it is this very detail of the "multi-ported memory" implementation which the present application disclosure addresses (62 of Fig. 6) to improve the cost, power, and performance of a given computer system with multiple host controllers (66, 68, 70) and client resources (76, 78, 79, 80, 82, 84, 86, and 64 of Fig. 6 of the present application).

Claims 2 and 12 of the present application are different from those described by MacLellan at col. 12, lines 41 et seq.; Fig. 8; col. 14, lines 12 to col. 15, lines 1, and memory controller logic sections 5010, col. 18, lines 42-55, which describe a "cached-memory" with "TAGs" for memory board and slot locations. As described above, the present application describes the circuit switched crossbar bus, whereas MacLellan describes a packet switched network implementation.

Claims 3, 13, and 22 of the present application are different from those described by MacLellan's crossbar switch (5004), col. 18, lines 5 et seq., and resource arbitration controller, Fig. 10, col. 19, lines 11 et seq.; col. 23, lines 26 et seq., in that the present application describes the point-to-point "connection" of non-blocking bus wires, whereas MacLellan describes a packet "routing" as can be seen from the details of Fig. 11A-D and Fig. 12A-D which describes the functional blocks of Fig. 10, the crossbar (5004).

Claims 8, 18, and 24 of the present application are different from those described by MacLellan's peripheral resources (140) and peripheral controller (260), in that the present application provides a circuit switching crossbar to connect the host processor to the peripheral devices for instant access. In contrast MacLellan describes a method of connecting a host to a peripheral device through a packet switching network coupled by a large set of "shared cache memory" (220). MacLellan speaks of a crossbar of serial packets (col. 14, lines 35-40, 57 to

col. 15, line 5; col. 18, lines 50-53; col. 20, lines 58 to col. 21, line 2) of parallel access, but not of simultaneous - single cycle accesses.

Claims 9, 19, and 25 of the present application are different from those described by MacLellan's crossbar switches (col. 18, lines 5 et seq.) and arbitration controller (Fig. 10; col. 19, lines 11 et seq.; col. 23, lines 26 et. seq.), in that the present application provides a bus arbitration controller that switches the circuit for the processor to connect directly to peripherals, whereas the MacLellan arbitration controller routes the packets to different peripherals via a centralized shared buffer memory (220).

Claim 27 is different from MacLellan's system because MacLellan describes a packet switched network of redundant memory subsystems for a fault tolerant computer using Dual-Ported Memory. The present application describes the implementation of multi-ported memory and peripheral devices via a circuit switched crossbar bus architecture.

The Office Action rejects claims 1-3 under 35 U.S.C. 102(b) as anticipated by Srini (U.S. Patent 5,053,942).

The present application is significantly different from Srini because the crossbar implementation of the present application utilizes circuit switched point-to-point bus topology (130, 134, 128, 132 of Fig. 7 of the present application), whereas Srini describes the tristate buffer switches (510, 511, 512 of Fig. 7 of Srini) on cross-point bus matrix topology (502, 504 of Fig. 6 of Srini).

The Office Action rejects claims 1-3, 8-9, 11-13, 18-19, 21-22, 24-25 and 27 under 35 U.S.C. 102(e) as anticipated by Goodwin. Goodwin does not teach or suggest the present invention as claimed, nor would it have been obvious for someone to expand the crossbar switch of the Goodwin patent to invent the crossbar resource architecture of the present application.

Goodwin describes an embodiment (col. 4, lines 49-56) where a crossbar is connected to multiple memory blocks and a CPU, but Goodwin does not describe a possibility of having multiple IO devices and arbitration modules. On the contrary, Goodwin's IO and arbitration modules are not the main part-of the crossbar data path. Rather, they are a central arbiter and a default fall-out path for the non-existing memory targets.

Goodwin does not teach how the crossbar could be developed. It simply uses the term "crossbar" as a means to describe a non-blocking interconnect mechanism to access interlaced memory banks (col. 6, lines 43-49; col. 7, lines 9-12; col. 7, lines 20-24; col. 7, lines 55-58; col. 7, lines 65-67) for multiple host to improve cache latency and data coherency by utilizing the staggered memory access to "interleaved" memory blocks for cache line fills and "victim" line writes (col. 8, lines 33-38 of Goodwin).

The Office Action rejects claims 1-2, 11-12, 21, and 24 under 35 U.S.C. 102(b) as anticipated by Hiller (U.S. Patent 5,081,575). Hiller does not teach or suggest the present invention as claimed, and it would not have been obvious to expand Hiller's crossbar memory topology to include other system resources, because, Hiller also speaks of crossbar linkage to highly parallel "interlaced memory banks" (8 of Fig. 1 of Hiller) as can be seen from the data storage allocation map (Fig. 3 of Hiller) for improved memory access performance. Note that the consecutive data words are sequentially allocated along PMEM0 to PMEM7 and so forth (Figs. 4-7) and provide a pipelined data access to stagger the memory access cycle stages to increase effective data throughput as can be seen from the timing diagrams (Fig. 13).

Section 103 Rejections

The Office Action rejects claims 3-4, 13-14, 22-23 and 25-26 under 35 U.S.C. 103(a) as unpatentable over Hiller in view of Goodwin; rejects claims 4-7, 10, 14-17, 20, 23 and

26 under 35 U.S.C. 103(a) as unpatentable over MacLellan in view of Official Notice, and rejects claims 4-7, 10, 14-17, 20, 23 and 26 under 35 U.S.C. 103(a) as unpatentable over Goodwin in view of Official Notice. In view of the above explanations showing that neither Hiller, Goodwin, nor MacLellan describes the required elements of the present application, they cannot be combined to teach or suggest the present invention as claimed.

Applicant further points out that all the prior art cited centers around a crossbar application for memory array applications. in explanation and response to Section 7 of the Office Action, both Hiller and Goodwin describe the crossbar switch as "interlaced" memory block applications - to specifically hide the access time of the memory subsystem via pipelined access for cache line fills and processing of sequential data.

In reference to Section 8 of the Office Action, MacLellan speaks of a packet switching network and Hiller speaks of interlaced memory banks, and neither addresses the need of utilizing crossbar architecture to improve overall systems performance (not just processor execution speed, not just memory access latencies, and not just pipelined cache line fills, but to resolve a performance bottleneck) by decoupling the high speed memory banks and low speed peripheral controllers with a non-blocking resource controller in embedded processor applications.

Consequently, all of the prior art utilizes the crossbar to accelerate the processor performance by increasing the apparent memory access bandwidth, whereas the present invention utilizes the circuit switched crossbar architecture to uniquely accommodate slow speed peripherals in the midst of high speed memory devices to improve system performance and system efficiency where both slow and fast devices must coexist. Applicant believes this concept is novel and non-obvious.

CONCLUSION

Applicant has explained the differences between the claims and the cited references, and believes the claims are in condition for allowance.

If any further questions should arise prior to a Notice of Allowance, the Examiner is invited to contact the attorney at the number set forth below.

Respectfully submitted

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on June 30, 2004, by Diana Dearing.

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